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1 On static compaction of test sequences for synchronous sequential circuits   ▬

Irith Pomeranz, Sudhakar M. Reddy
June 1996 **Proceedings of the 33rd annual conference on Design automation**
Publisher: ACM Press
Full text available: 📄 pdf(60.62 KB)   Additional Information: full citation, references, citings, index terms

2 An approach to test compaction for scan circuits that enhances at-speed testing   ▭

Irith Pomeranz, Sudhakar Reddy
June 2001 **Proceedings of the 38th conference on Design automation**
Publisher: ACM Press
Full text available: 📄 pdf(87.48 KB)   Additional Information: full citation, abstract, references, citings, index terms

We propose a new approach to the generation to compact test sets for scan circuits.
Compaction refers here to a reduction in the test application time. The proposed
procedure generates an initial test set that is likely to have a low test application time. It
then applies an existing static compaction procedure to this initial test set to further
compact it. As a by-product, the proposed procedure also results in long primary input
sequences, which are applied at-speed. This contributes to ...

3 Procedures for static compaction of test sequences for synchronous sequential circuits based on vector restoration   ☐

R. Guo, I. Pomeranz, S. M. Reddy
February 1998 **Proceedings of the conference on Design, automation and test in Europe**
Publisher: IEEE Computer Society
Full text available: 📄 pdf(47.20 KB)   Additional Information: full citation, abstract, references, citings, index terms
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We propose several compaction procedures for synchronous sequential circuits based on
test vector restoration. Under a vector restoration procedure, all or most of the test
vectors are first omitted from the test sequence. Test vectors are then restored one at a
time or in subsequences only as necessary to restore the fault coverage of the original
sequence. Techniques to speed-up the restoration process are investigated. These include
limiting the test vectors initially omitted from the test se ...

Keywords: static test compaction synchronous sequential circuits